

# Slater & Matsil, L.L.P.

Suite 1000  
17950 Preston Road  
Dallas, Texas 75252  
Phone: (972) 732-1001 Facsimile: (972) 732-9218

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TO: Examiner Nathan Ha  
U.S. Patent & Trademark Office

FAX NO.: (571) 273-1707

FROM: James C. Kesterson  
Slater & Matsil, L.L.P.

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RE: **Applicant:** Lee, et al.  
**Serial No.:** 09/988,183  
**Date Filed:** November 19, 2001  
**Docket No.:** 2001 P 11904 US  
**Art Unit:** 2814  
**Title:** Formation of Dual Work Function Gate Electrode

### SUPPLEMENTAL AMENDMENT AFTER FINAL REJECTION

Per your conversation with Jim Kesterson today, below please find a revised abstract for the above referenced case:

A method of manufacturing a dual work function gate electrode used with a CMOS structure. Penetration of the boron doping material into the channel region is suppressed without causing boron depletion near the gate oxide region by laser annealing a layer of a- Si covering poly- Si and the gate oxide at its nMOS site and the pMOS site. The laser annealing is accomplished at an energy level sufficient to melt a portion of the a- Si, but insufficient to melt the poly- Si. Avoiding melting of the poly- Si reduces gate oxide damage.

The abstract has been rewritten in compliance with proper U.S. Patent Office Procedure.

  
James C. Kesterson 25,882  
Attorney for Applicants